FA 8.1: Low-Jitter and Process-Independent DLL and PLL Based on Self-Biased Techniques

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Growing demand for high-speed I/O on digital ICs creates an increasingly noisy environment in which phase-locked loops (PLLs), delay-locked loops (DLLs), and other clock generating blocks must function. This noise, typically in the form of supply noise and substrate noise, makes design of low-jitter PLLs and DLLs challenging. This paper describes both a DLL and PLL design based upon self-biasing techniques in which all bias voltages and currents are referenced to other generated bias voltages and currents. Self biasing leads to a number of desirable properties that include IC process independence, fixed damping factor, fixed bandwidth-to-operating-frequency ratio, broad frequency range, input phase offset cancellation, and, most importantly, low input tracking jitter. Both damping factor and bandwidth-to-operating-frequency ratio are determined completely by a ratio of capacitors.

The voltage-controlled delay line (VCDL) and the voltage-controlled oscillator (VCO) used in the two designs are based upon differential-buffer delay stages with symmetric loads and replica-feedback biasing as shown in Figures 1 and 2 [1]. These buffer stages have about 0.25%/V supply noise rejection operating over a broad delay range with low supply voltage requirements that scale with the operating delay. They operate with a delay that varies inversely proportionally to the control voltage and with internal bias currents that vary inversely proportionally to the square of the operating delay.

The DLL design, shown in Figure 3, uses the buffer bias current as the charge pump current. In a conventional DLL design, the loop bandwidth is a constant fraction of the operating frequency when both the VCDL gain (s/V) and the phase comparator/charge pump gain (A/rad) are constant. When the symmetric load buffer stages implement the VCDL, the loop bandwidth varies inversely proportionally to the operating frequency, which is undesirable. However, if the buffer bias current is used as the charge pump current, the loop bandwidth is represented by:

$$\omega_N/\omega_{REF} = (1/2\pi)(I_{CH}/C_1)(K_{DL}) = (x/4\pi)(C_B/C_1)$$

where I_{CH} is the charge pump current, K_{DL} is the VCDL gain, x is the set ratio of the charge pump current to the buffer bias current, C_B is the total effective load capacitance for all buffer stages, and C_1 is the filter capacitance. The key results are that the ratio of the loop bandwidth to the operating frequency is constant and completely determined by a ratio of easily matched capacitances and that the DLL can operate over the same broad frequency range achievable by a VCO based on the same buffer stages operating open loop.

The PLL design, shown in Figure 4, uses the buffer bias current as the charge pump current and a symmetric load as the filter resistor. For a conventional PLL design, the loop bandwidth is fixed and independent of operating frequency when both the VCO gain (Hz/V) and the phase comparator/charge pump gain (A/rad) are constant [2]. The minimum operating frequency of the PLL is limited to about a decade above the loop bandwidth for stability. In addition, the input tracking jitter is inversely proportional to the loop bandwidth when the PLL is exposed to low-frequency supply or substrate noise. Conservatively setting the loop bandwidth low and damping factor high to insure adequate phase margin over all process variations and operating conditions leads to poor jitter performance. However, if the buffer bias current is used as the charge pump current and a symmetric load is used as the filter resistor, the damping factor and loop bandwidth are represented by:

$$\zeta = 1/2\sqrt{(I_{CH}K_V R^2 C_1)} = (1/4y\sqrt{x})\sqrt{(C_1/C_B)}$$

$$\omega_N/\omega_{REF} = 2\zeta/(RC_1\omega_{REF}) = (\sqrt{x}/2\pi)\sqrt{(C_B/C_1)}$$

where K_V is the VCO gain (Hz/V), R is the filter resistance, and y is the set ratio of the filter resistance to the symmetric load resistance. Similar to the DLL, the ratio of the loop bandwidth to the operating frequency and the damping factor are both constant and completely determined by a ratio of capacitances. In addition, the PLL can operate over a broad frequency range identical to the open loop frequency range achievable by the VCO. The filter resistor is actually the output resistance of the bias generator for the control voltage output. The charge pump current is replicated at both the input and output of the bias generator so that the current is applied to both the filter capacitor and resistor [3].

DLLs and PLLs that use conventional charge pump designs typically have input phase offsets that change with operating frequency and process variations. This dependence results from a varying Thevenin equivalent output voltage. The charge-pump circuit shown in Figure 5 is based on the symmetric load buffer stage design and has a Thevenin equivalent output voltage equal to the control voltage when both U and D inputs are asserted. This Thevenin voltage equivalence, along with the extra devices to balance the switching charge injection, completely balances the charge pump and results in zero input phase offset.

The architecture of the DLL, illustrated in Figure 6, mirrors the design in Reference 4 to allow it to perform frequency synthesis and duty cycle correction with one key difference. The design in Reference 4 uses a single delay chain to form a VCO that is continuously synchronized by a single reference input edge type. This delay chain must include any necessary differential to single-ended conversion and chip-wide clock distribution within a half-cycle time budget. The jitter produced by the clock distribution will be multiplied by twice the clock multiplication factor as observed in the tracking jitter. The DLL design presented here uses two DLLs. The first DLL performs frequency multiplication and can be completely based on differential buffer stages with high supply-noise rejection. The second DLL performs phase synchronization and can span any number of cycles.

The DLL and PLL are fabricated on a 0.5μm n-well CMOS gate array process. A micrograph of the DLL and PLL is shown in Figure 7. PLL jitter with 500mV of 1MHz square wave supply noise is illustrated in Figure 8. Performance of the DLL and PLL are summarized in Tables 1 and 2 respectively. The measured jitter is increased by the gate array implementation of the filter capacitor which has interleaved rows of nMOS devices that lead to control voltage coupling to ground. The PLL operates from 0.0025MHz to 550MHz and has 384ps tracking jitter at 250MHz with 500mV supply noise.

References:

[1] Maneatis, J., M. Horowitz, "Precise Delay Generation Using Coupled Oscillators," IEEE J. Solid-State Circuits, vol. 28, no. 12, pp. 1273-1282, Dec., 1993.

[2] Young, I., et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," IEEE J. Solid-State Circuits, vol. 27, no. 11, pp. 1599-1607, Nov., 1992.

[3] Mijuskovic, D., et al., "Cell-Based Fully-Integrated CMOS Frequency Synthesizers," IEEE J. Solid-State Circuits, vol. 29, no. 3, pp.271-279, March, 1994.

[4] Waizman, A., "A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," ISSCC Digest of Technical Papers, pp. 298-299, Feb., 1994.

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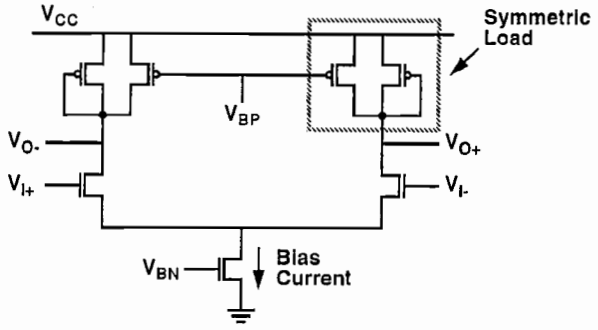

Figure 1: Differential buffer delay stage with symmetric loads.

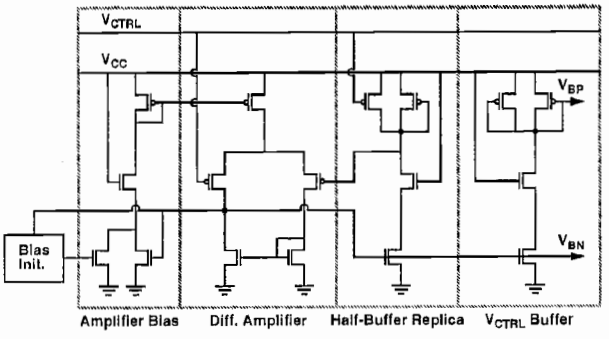

Figure 2: Replica-feedback current source bias circuit.

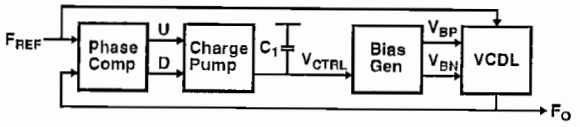

Figure 3: DLL block diagram-clock distribution omitted.

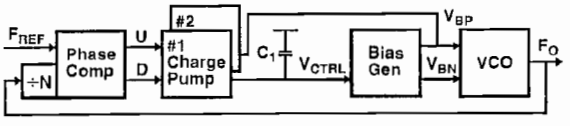

Figure 4: PLL block diagram-clock distribution omitted.

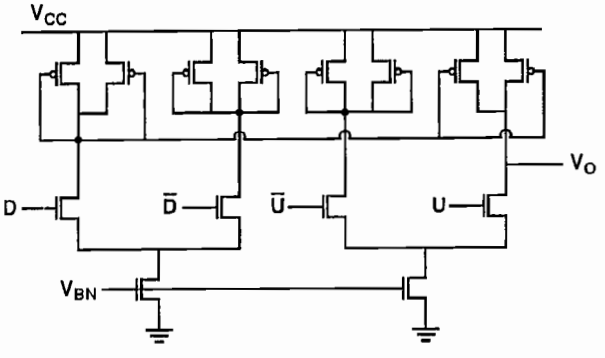

Figure 5: Offset-cancelled charge pump with symmetric loads.

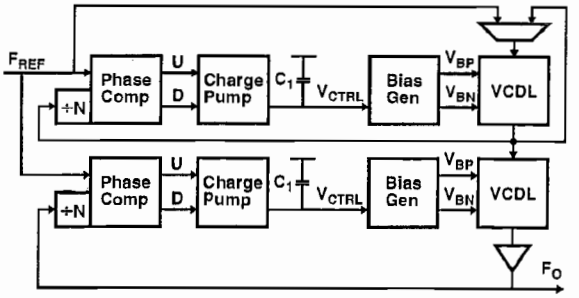

Figure 6: Complete dual-loop DLL block diagram.

Figure 7: See page 430.

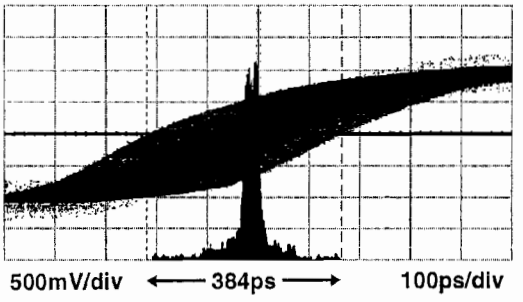

Figure 8: Measured PLL tracking jitter with 500mV supply noise.

Operating frequency range:	0.0025MHz - 400MHz at 3.3V
Minimum supply requirements:	2.45V, 8.6mA
Input offset, sensitivity:	112ps, <100ps/100MHz
Tracking jitter, sensitivity:	610ps, 1165ps/V (P-P)
Cycle-to-cycle jitter, sensitivity:	262ps, 430ps/V (P-P)
Block area:	1.18mm^2
Technology:	0.5μm n-well CMOS gate array

Table 1: DLL performance characteristics measured at 250MHz with 500mV 1MHz square-wave supply noise.

Operating frequency range:	0.0025MHz - 550MHz at 3.3V
Minimum supply requirements:	2.10V, 4.4mA
Input offset, sensitivity:	<25ps, <10ps/100MHz
Tracking jitter, sensitivity:	384ps, 704ps/V (P-P)
Cycle-to-cycle jitter, sensitivity:	144ps, 290ps/V (P-P)
Block area:	1.91mm^2
Technology:	0.5μm n-well CMOS gate array

Table 2: PLL performance characteristics measured at 250MHz with 500mV 1MHz square-wave supply noise.

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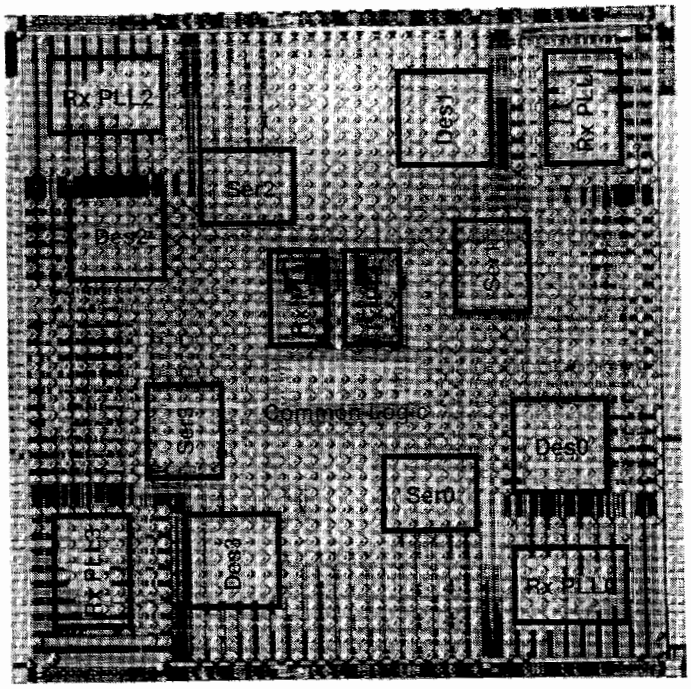

Figure 6: Chip micrograph.

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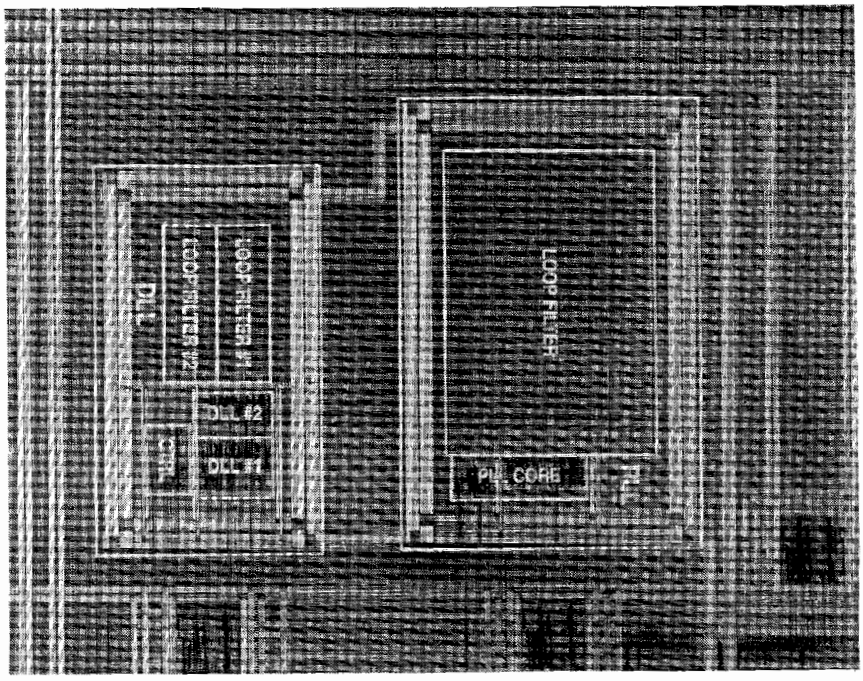

Figure 7: DLL and PLL die micrograph.