A Better Low-jitter Digital PLL

A new, state-of-the-art digital control algorithm

By Can Wang and Brian Gardner
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Summary

True Circuits has added a state-of-the-art digital control algorithm to its flagship, low-jitter, digital LC PLL, the Ultra. TCI added this logic in collaboration with Stanford VLSI group. The new control loop cuts the lock time by as much as 70%, while directly controlling the loop bandwidth accurately.

The Ultra PLL already provides extremely low jitter, very small size, low power and multiplication factors over 250,000, as well as 26 fractional bits. It has been in production for over eight years in a variety of high-performance products.

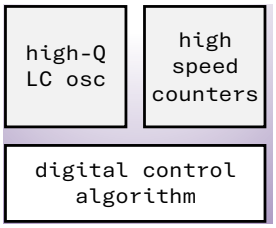
This new control algorithm was added using carefully guided, but conventional place-and-route technology. With this technology added to TCI's arsenal of high-productivity tools, the new flow opens the door for an expansion of the product portfolio, and for customers to add their own features.

A New Control Algorithm

Our innovative digital PLL control algorithm achieves unprecedented loop bandwidth precision, enabling user-defined settings as accurate as 0.1% of Fref – with further accuracy scaling available on demand. Critically, this precise bandwidth is maintained consistently across PVT variations through continuous background loop-gain calibration. This eliminates performance drift, ensuring stable PLL dynamics (lock time, jitter tolerance) without manual intervention under any operating condition.

Integrated correlated noise and spurious measurement circuits provide active immunity against environmental disturbances. By continuously monitoring and analyzing correlated noise components, the PLL guarantees stable operation even in excessively noisy environments. This built-in intelligence distinguishes external threats from intrinsic noise, delivering unmatched resilience for mission-critical clocking applications.

Adding to a First of Its Kind, the Ultra PLL

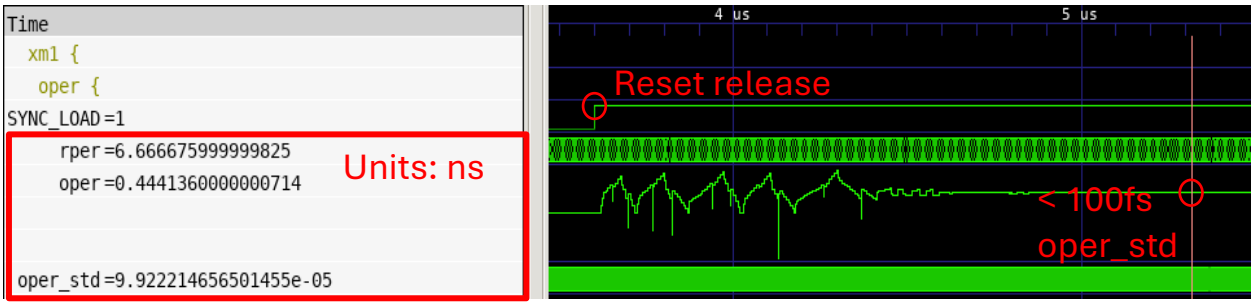


The original Ultra PLL is the most sophisticated PLL in the world, offering unprecedented operating range, extremely high performance and a huge frequency range: multiplication factors from 1 to over 250,000 to support references from 32KHz to 1GHz. It has precise frequency control with 26 fractional bits for extremely high fractional-N resolution. Using a high-Q, LC oscillator, the PLL has low jitter (<500fs) for the most demanding SerDes and ADC reference clocks. It can also generate precise and adjustable frequency spreading with programmable rate and depth to meet tight FCC requirements.

Compared to the competition, the Ultra PLL is 1/5 the size, lower power and has many one-of-a-kind features referenced above. By adapting the internal division ratio to match the LC VCO's natural frequency, the new control loop enables wide output frequency coverage without demanding a large tuning range LC tank. This allows the use of a compact, very high-Q LC tank, which results in a significant improvement in jitter performance (<100fs) over the original design, while maintaining its small size, low-power and programmability.

A Peek into Performance

With the addition of the new digital control algorithm and other enhancements, the Ultra PLL has truly impressive performance. Following extensive simulation and circuit optimization, the performance shown below was achieved. A test chip has been taped out in order to validate the many performance improvements shown in simulation.



Ref Clock Rate	150 MHz
Time taken to get RMS jitter < 100fs	1.5 us
Cycle taken to get RMS jitter < 100fs	~250
Steady-state RMS jitter	< 100 fs

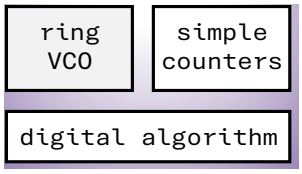
*Subject to measurement condition and noise profile

Building on TCI's Unique Development Flow

The new control logic was created using conventional, digital place and route. This approach adds to True Circuits' JSPICE™ Design Environment (JDE™) development flow that already uses unique analog and high-speed digital cells that are placed algorithmically, while maintaining the control needed for critical circuits.

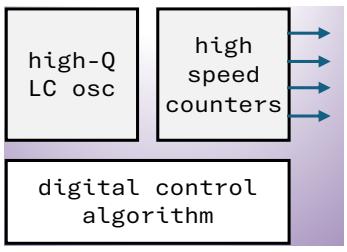
Using carefully controlled conventional tools along with JDE, TCI will build the expanded portfolio of PLLs and DLLs shown below. In addition, customers can be provided synthesizable or hardened IP with a modular design so that they can build their own features easily and safely using hard macros and stock Verilog code.

Micro PLL



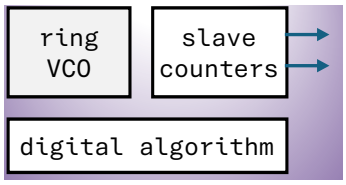
* Small and synthesizable general purpose PLL
* Multiplies the reference clock by any integer or fractional-N value from 1 to 500K
* Supports reference clock frequencies as low as 32KHz and output frequencies as high as 3GHz
* Stays locked to the reference clock while it changes over a 10:1 frequency range
* Very fast locking and quickly restarts from sleep mode

Precision PLL



* Generates multiple precision clocks supporting any modulation scheme from almost DC to 10GHz
* Output clocks can be independently, dynamically programmed cycle-by-cycle to any clock period
* Output clock frequencies can be a precise ratio of a floating point number times the reference frequency
* Integrated phase noise is better than 500fs RMS
* Ideal for SerDes, processor and DVFS applications

Micro DLL



* Small synthesizable DLL with a master and multiple slave topology
* Supports reference frequencies of 500MHz to 3GHz
* Reference changes over an 8:1 frequency range while providing 9-bit accuracy in slave delay programming
* Slave delays can be changed glitch-free and the DLL quickly restarts from a sleep mode
* Very small, precisely cancelled zero offset

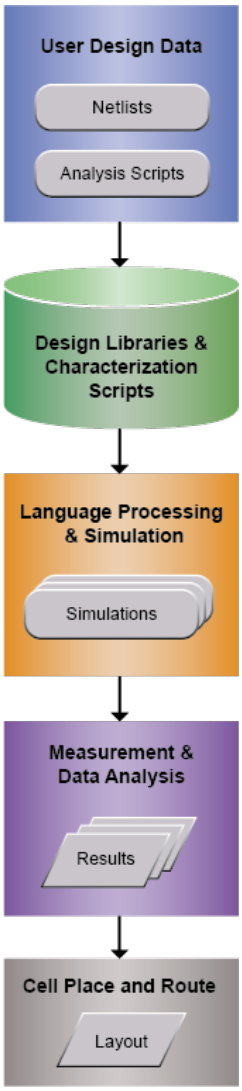
JSPICE™ Design Environment (JDE™)

The JSPICE Design Environment (JDE) is a robust simulation and design environment that streamlines the creation and characterization of complex AMS circuits. Created using modern design and software practices, it enables a revolution that promises to cut development time by 90%

JDE can create and run unlimited parallel simulations, and has powerful functions to distill the large results into simple plots or tables. JDE incorporates text, processing code and scripts that move analog design into the realm of modern software.

JDE moves mostly hand-drawn layout to cell-based layout without losing the layout control needed for critical circuits. The JDE design database contains careful cell placement information that allows routing to be done automatically. The bulk of the layout porting effort is thereby reduced to building and characterizing a set of cells. JDE automatically characterizes the cells.

More information about JDE can be found at http://www.truecircuits.com/jspice.html.



All data needed for the design definition and testing is here.

Data analysis scripts utilize a large set of measurement and data reduction functions to simplify the automation of circuit characterization.

Design libraries contain logic and arithmetic circuits, stimulus and language extensions to simplify the expression of designs.

User- and pre-defined characterization scripts make it easy to automate circuit characterization.

The JSPICE language used in the design is preprocessed to create a very fast executable design generator.

Parallel simulations, one for each user-specified netlist parameter combination, are run locally or in the cloud.

Powerful waveform analysis language and data reduction programs distill data into human understandable results (numbers, plots, reports) and data to feed into other simulations.

High-speed analog and digital designs can be deterministically placed and routed allowing them to be process independent.

JDE™
JSPICE™ DESIGN ENVIRONMENT

Can Wang is currently a Ph.D. candidate at Stanford University and an engineering intern at TCI. His interests are in SerDes, clocking systems and exploring analog/mixed-signal design methodology. He holds several academic publications in VLSI and JSSC.

Brian Gardner is TCI's V.P. of Business Development. He is a long time semiconductor industry veteran, and has spent much of the last 25 years in the semiconductor IP market. He has held senior positions in general management, marketing and business development at Canaan, Denali, Cadence, QLogic and Motorola; as well as chip startups Interactive Silicon and OmegaBand. As General Manager of the microcontroller division at Motorola, he helped build the 68HC05 microcontroller into a dominant architecture with sales of more than three billion units. Brian holds a B.S. degree in Electrical Engineering from LSU.

True Circuits, Inc. is a leading provider of high-speed mixed-signal analog IP. It was founded in 1998 with headquarters in Los Altos. True Circuits builds easy to use, highly programmable hard macros, like Phase-Locked Loops, Delay-Locked Loops, and DDR PHYs, in most foundries and process variants. True Circuits has an experienced mixed-signal design team and close technical relationships with major foundries. Its customers include most semiconductor suppliers and design service providers. Over the 27 years that it has been in business, True Circuits has shipped countless IP blocks used on billions of chips in about 100 process variants.