

▶ PRODUCT SUMMARY

IP DESIGN TYPES

CLOCK GENERATOR PLL

- Designed as a very flexible clock multiplier capable of multiplying an input clock from 1 to 4096 with small period jitter while operating at the highest possible bandwidth.
- Delivers optimal performance over all multiplication settings.
- Optionally provides multi-phase outputs and 4 bits of precise fractional-N control.
- Ideal for system clock generation and video clock applications.

GENERAL PURPOSE PLL

- Designed as a wide range clock multiplier with deskew capability.
- Delivers optimal performance over all multiplication settings.
- Low area and low power.
- Suitable for system clock and general purpose applications.
- Ideal for cost sensitive applications.

ULTRA PLL

- New state-of-the-art architecture using high-speed digital and analog circuits that offers unprecedented operating ranges and extremely high performance.
- Ultra low jitter performance for the most demanding SerDes and ADC reference clocks.
- Ultra wide frequency range with multiplication factors over 250,000 to support 32KHz to 1GHz references.
- Precise frequency control with a least 26 fractional bits (at least 10 precise) for extremely high fractional-N resolution.
- Optional spread spectrum support with programmable rate and depth to meet tight FCC requirements.
- Low power and compact size.
- Highly programmable so one PLL can be used for all applications on a SoC.

SPREAD SPECTRUM PLL

- Designed for PC, networking, and consumer electronics applications where spread-spectrum clock sources are required to satisfy FCC requirements for peak RF spectral emissions.

- Bandwidth, spreading rate, and spreading amount are precisely adjustable to allow the designer to dial-in the desired characteristics.
- Feedback divider with 8 fractional bits allows the frequency to be set more precisely when the bandwidth is reduced.

IoT PLL

- Designed for very low power, running completely from core power.
- Supports 32KHz reference clocks.
- Extremely wide range of operation with multiplication factors over 8,000.
- Small area, delivered as a single hard macro with guardrings and isolation.
- Flexible and highly programmable.
- Ideal for low power and cost sensitive applications such as IoT wearables and remote sensors.

DESKEW PLL

- Designed to eliminate clock distribution latency in systems and individual chips.
- Precisely aligns the clock distribution output with a reference clock.
- Provides a zero-delay feedback divider and zero-skew divided clock outputs.

DDR DLL

- Analog master-slave DLL designed for high-speed DDR-style interface applications.
- Generates precise delays that can be programmed from 0 to 360 degrees of the reference period.
- Delays multiple periodic or aperiodic signals independent of voltage and temperature.
- Delivers optimal performance over a wide frequency range.
- Available in different form factors and slave counts.

MULTI PHASE DLL

- Designed for high-speed interface applications.
- Generates precise multi-phase clocks directly from the reference clock.
- Delivers optimal performance over a wide frequency range.

IP SELECTION GUIDE

APPLICATION	FUNCTIONALITY	RECOMMENDED PRODUCT(S)
Core Clocking	Fast Clocking	Clock Generator PLL
Core Clocking	High Fout Resolution	Clock Generator PLL, Spread Spectrum PLL
Core Clocking	Slower Clocking	General Purpose PLL
Core Clocking	Deskew	General Purpose PLL, Deskew PLL
Core Clocking	Small Size	General Purpose PLL
Core Clocking	Spread Spectrum	Spread Spectrum PLL
Core Clocking	Fractional-N	Spread Spectrum PLL
Core Clocking	Ultra Low Jitter	Ultra PLL
Core Clocking	32KHz Reference	IoT PLL, Ultra PLL
DDR	Delay Lines	DDR DLL, Ultra PLL, Clock Generator PLL
ONFI	Delay Lines, Multiphases	Multi Phase DLL, DDR DLL
PCIe	Reference Clock	Ultra PLL
USB	Reference Clock	Ultra PLL
Ethernet	Reference Clock	Ultra PLL
IoT	Clock Generation	IoT PLL, General Purpose PLL

AVAILABILITY AND DELIVERABLES

- All IP designs available in TSMC, UMC and GLOBALFOUNDRIES processes from 180nm to 7nm.
- GDSII and LVS Spice netlists.
- Behavioral, synthesis and LEF models.
- Extensive user documentation.
- Integration and testing support to insure successful tape outs.

LICENSING

- Sales directly through True Circuits, a variety of design services companies and global sales reps.
- Per use license fees with no product royalties.
- Standard license agreement.
- Pricing and complete datasheets available under mutual NDA.
- Contact True Circuits Sales at sales@truecircuits.com.

ABOUT TRUE CIRCUITS

True Circuits, Inc. offers a complete family of standardized, silicon-proven PLL and DLL hard macros that spans nearly all performance points and features typically requested by ASIC, FPGA and SoC designers. True Circuits utilizes robust state-of-the-art circuits, a methodical and proven design and test strategy, and close associations with the major foundries. True Circuits' PLL and DLL product portfolio is available in most TSMC, UMC and GLOBALFOUNDRIES processes and process variants from 180nm to 7nm.

Since 1998, True Circuits has distinguished itself as the technology leader in the timing IP space, and its PLLs and DLLs are used extensively around the world in its customers' products with production volumes in the billions.