Phase-Locked Loops Demystified

by John G. Maneatis and Eskinder Hailu

Over the past decade, Phase-Locked Loops (PLLs) have become an integral part of the modern ASIC design. PLLs provide the clocks that sequence the operation of the various blocks on an ASIC chip as well as synthesize their communications. There are various types of PLLs targeting specific applications. Clock generator PLLs are capable of large frequency multiplication. They are primarily used to generate clocks for digital logic. Deskew PLLs are used to eliminate clock skew between two clock domains. They are often used in older synchronous chip-to-chip IO applications. Spread spectrum PLLs slowly vary the clock frequency in order to spread a clock's electro-magnetic (EM) signature over a frequency band, thereby reducing the maximum emitted EM power at any frequency. Spread spectrum PLLs are used in many consumer products such as PCs, PDAs, etc. It is essential that PLLs be carefully specified, designed, and verified. A poorly designed or improperly used PLL can cause substantial delay in product launch or, in the worst case, total product failure.

PLL architectures are generally grouped into two categories: wide-band and narrow-band. These definitions are mainly based on the voltage controlled oscillator (VCO) topologies implemented. Narrow-band PLLs generally employ the resonant characteristic of inductors and capacitors to create the VCO. They are typically used in communications applications that place stringent long-term jitter requirements on the PLL. The improved long-term jitter performance of narrow-band PLLs is offset by the narrow frequency tuning range. Typically the tuning range is only 10-20% of the center frequency. A large chip area is also consumed in realizing the inductors. Furthermore, the inductance value will vary from chip to chip as a result of variations in the manufacturing process. The combination of narrow tuning range and varying inductance value necessitates extensive characterization of the VCO to ensure the target frequency range can be met across all operating PVT (process, voltage, temperature). Wide-band PLLs avoid using on chip inductors. The VCOs are commonly built as ring or relaxation oscillators, which use RC delays to establish the clock period. These PLLs have the benefit of a large frequency tuning range (Fmax/Fmin >10X), relatively small on-chip footprint, and potentially low power. However, these benefits are offset by the inferior long-term jitter characteristics of such PLLs. Hence, wide-band PLLs are seldom used in applications with stringent long-term jitter requirements.

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A typical PLL architecture is shown in Figure 1.

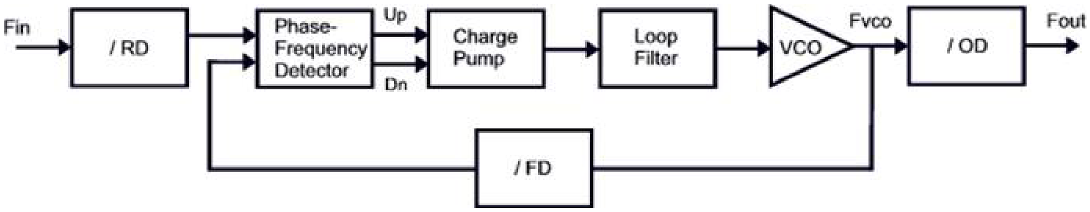

Figure 1

The relationship between the output and input frequency is given by:

Fout= Fvco/OD, and
Fvco= Fin*FD/RD, where:

RD is the reference clock divider,
FD is the feedback divider,
OD is the output divider,
Fin is frequency of the reference clock,
Fvco is frequency of the VCO, and
Fout is the frequency of the output clock.

PLLs are typically modeled as second or third order feedback systems. Some of the key PLL system parameters are: natural frequency or loop bandwidth (Wn), damping factor (zeta), and the 3-dB bandwidth (3-dB BW) which is proportional to Wn*zeta. The lock time of the PLL is proportional to 1/(3-dB BW).

Other important system parameters of the PLL include static and dynamic supply noise sensitivity, power dissipation, area, duty cycle of the output clock, static phase offset, and of course, long-term and short-term jitter.

The PLL shown in Figure 1 is inherently a sampled data system as it only compares reference and feedback edges. For the loop to remain stable, its loop bandwidth, Wn, has to adhere to the following relationship: Fin/(RD*Wn) > 10. For a fast and stable transient response of the loop, the damping factor is typically kept between 0.7 and 1.

Assuming a noise-free reference clock, one of the main contributors to the long-term jitter in wide-band PLLs are the VCOs themselves. The main contributors to short-term noise are reference frequency spurs in the output clock frequency spectrum, created as a result of charge pump current mismatches, charge injection and static phase offsets. For a given VCO frequency, Fvco, increasing Wn will track out more of the noise introduced by the VCO and reduce the long-term jitter. Increasing Wn will also reduce the lock time of the PLL, improving its transient performance. Thus, FD should be kept as small as possible so that Wn is maximized.

Larger FD values can also result in increased short-term jitter. This increase is because a larger FD value corresponds to a reduced refresh rate in the loop filter. In the presence of leakage and other mismatches, a large FD can result in increased spurs. In addition to keeping FD small, spurs can be further reduced by increasing the order of the loop filter. However, increasing the order of the loop filter will reduce Wn resulting in increased long-term jitter. The above discussions indicate the existence of a tradeoff between long-term and short-term jitter in PLLs.

In addition to low jitter, the PLL should also have optimal transient response across all PVT. To achieve this result, zeta should remain relatively constant across PVT. However, using static control pins to bias the PLL for optimal Wn and zeta across all PVT is impossible, since the PLL parameters that determine Wn and zeta can show up to 2X variation over PVT. To address this issue, such a PLL would need to be designed conservatively and would typically have low Wn and, subsequently, large long-term jitter.

One class of PLLs, called self-biased PLLs, relax the constraints that require a lower loop bandwidth. They work by biasing a PLL at its optimal point across all PVTs. This is achieved by using internal feedback to sense the PLL settings and vary the bias points accordingly for optimal performance. In addition, these PLLs can use specialized filters that can eliminate spurs, significantly relaxing the long-term/short-term jitter tradeoff. For details on self-biased PLLs, please refer to the following references [1,2], available at: http://www.truecircuits.com/white_papers.html.

Employing the above principles, TCI provides robust, high multiply range (1-4096), low jitter, and low power PLL hard macros in TSMC, UMC, Chartered and Common Platform processes from 0.25um to 55nm. Please check our product portfolio at: http://www.truecircuits.com/product_matrix.html.

References

[1] Maneatis, et. al., "Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL," IEEE Journal of Solid-State Circuits, Vol. 38, No. 11, November 2003.

[2] Maneatis, et al., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996.

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