The JSPICE™ Design Environment (JDE™)

A revolution in high-speed analog and mixed-signal design

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The AMS Dilemma

The demand for high-speed analog and mixed-signal (AMS) designers is growing as the total market for AMS IP is predicted to double from 2024 to 2029 (Modor Intelligence.) Applications in AI, IoT, sensors and more depend on cutting edge AMS circuits. At the same time, AMS designers are aging and they are not being replaced by new college graduates.

Resolving this dilemma requires: 1) making existing designers much more productive and 2) creating tools that attract a new crop of designers and expedite their training.

Time for a Revolution: the JSPICE™ Design Environment (JDE™)

The JSPICE Design Environment (JDE) is a robust simulation and design environment that streamlines the creation and characterization of complex AMS circuits. Created using modern design and software practices, it enables a revolution that promises to cut development time by 90%.

This revolution is built around three paradigm shifts:

1. Massively parallel simulation
2. Modern text-based scripts and programming
3. Cell-based design and layout

Massively Parallel Simulation

JDE can create and run unlimited parallel simulations, and has powerful functions to distill the large results into simple plots or tables. These two advances unlock a new way to design. Rather than optimizing one parameter at a time by running a series of simulations, JDE can optimize three parameters over ten steps at all five PVT corners. The resulting 5,000 simulations are configured and launched quickly and automatically by JDE's fast cloud server. The measurement outputs are digested and simple and intelligible results are presented. A half day's work is done in ten minutes, and the work can be easily repeated later if the design changes. Massively parallel design is a paradigm change in thinking.

Modern Text-based Scripts and Programming

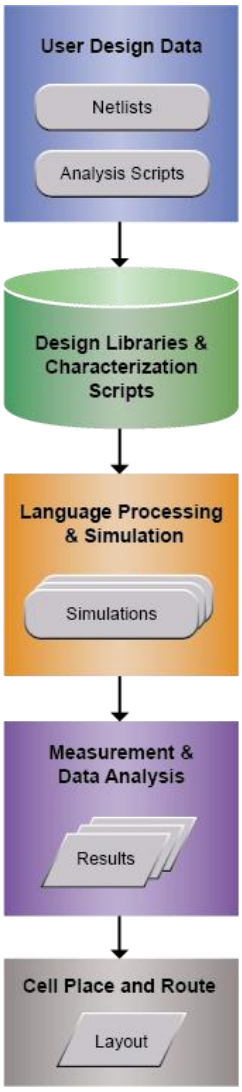
GUIs and schematics are a slow way to design. They resist automation. JDE incorporates text, processing code and scripts that move analog design into the realm of modern software. This may also help attract young software-savvy talent to the field of analog design.

Cell-based Design and Layout

JDE moves mostly hand-drawn layout to cell-based layout without losing the layout control needed for critical circuits. The JDE design database contains careful cell placement information that allows routing to be done automatically. The bulk of the layout porting effort is thereby reduced to building and characterizing a set of cells. JDE automatically characterizes the cells.

JDE in Detail

JDE is a collection of programs and scripts (100's) that acts on user specification and creates all the deliverables needed to integrate a design into an SoC: GDSII, RTL, .lib, etc. The user design netlist is written in text, and C code can be added to make the design highly configurable and express complex or repeated designs easily. The netlist design goes through a preprocessor program and becomes an executable that generates netlist(s) for simulation as well as inputs to create other views. The JSPICE mixed-mode simulator supports an unlimited number of simulations in parallel, controlled by the network processor, another part of JDE. The output of the simulations can be measured using waveform analysis tools that provide detailed insights into circuit behavior. Those measurements are then gathered and processed using data analysis functions into various readable results. Parametric simulation sweeps enable JDE users to create and distill tremendous amounts of data and quickly gain intuition into the design.



All data needed for the design definition and testing is here.

Data analysis scripts utilize a large set of measurement and data reduction functions to simplify the automation of circuit characterization.

Design libraries contain logic and arithmetic circuits, stimulus and language extensions to simplify the expression of designs.

User- and pre-defined characterization scripts make it easy to automate circuit characterization.

The JSPICE language used in the design is preprocessed to create a very fast executable design generator.

Parallel simulations, one for each user-specified netlist parameter combination, are run locally or in the cloud.

Powerful waveform analysis language and data reduction programs distill data into human understandable results (numbers, plots, reports) and data to feed into other simulations.

High-speed analog and digital designs can be deterministically placed and routed allowing them to be process independent.

JSPICE Preprocessing Language

The JSPICE input preprocessing language permits the expression of complex circuits through powerful extensions to the Berkeley SPICE and industry-standard SPICE input formats. These extensions include C statements and functions, multi-dimensional buses, signal structures and fully parameterizable sub-circuits. These features are needed to create a configurable design that can generate many different designs from a single database.

The language supports descriptions at various levels of abstraction, from abstract user definitions to transistor-level details. Directed synthesis and deterministic place and route complete the language's capabilities. The language is compiled and supports precompiled objects for very fast access to large design libraries and data sets.

Statistical Timing Analyzer

The preprocessor also includes a statistical timing analyzer that does a very comprehensive static timing analysis for the digital portions of a mixed-signal design. The analyzer defines gate functions for complete behavioral modeling. Gates are completely characterized, and the information is applied to the circuit, considering gate loading, edge rates and RC networks. The statistical timing analyzer can:

- Perform exact and statistical timing analysis
- Handle all clocked elements (FFs, latches, clocked gates, clocked MUXs)
- Handle arbitrary clock domains (synchronous and asynchronous)
- Automatically analyzes clock trees
- Automatically check asynchronous boundaries and multi-cycle paths
- Automatically calculate setup/hold time
- Support additional user defined timing checks
- Automatically perform structural checks
- Show exact timing paths for all delay differences
- Allow user to override timing information and the timing graph

JSPICE Core Simulator

The JSPICE core simulator is a significantly enhanced version of Berkeley SPICE. Fully compatible with all foundry SPICE models, it provides advanced features such as Verilog or behavioral modeling with delay-accurate timing, SPICE path simulations, Verilog A support, transient noise analysis, timestep control, multi-threaded execution, and compiled non-linear source evaluation. These enhancements put the JSPICE core simulator on par with industry-standard SPICE simulators.

JSPICE Cloud Server

The JSPICE cloud server allows users to run single simulations or thousands, even millions, in parallel with no additional effort. AWS™, Azure™, and Google Cloud™ are already supported. The server optionally supports a job scheduling interface similar to LSF to facilitate moving existing workloads. The server handles the task of scheduling simulation processes and transferring files and data to both local and cloud compute resources seamlessly. Local compute resources can be used efficiently for small jobs, while the cloud resources will be automatically allocated as needed within the user-defined limits.

Parametric Sweep Engine

The JDE parametric sweep engine can set up parallel simulation jobs sweeping through many parameters. It can run simulations with different top-level deck stimulus, perform overall calculations and data reduction, and even run additional simulations based on the results of previous simulations.

Waveform Measurement Engine

JDE includes a sophisticated waveform measurement engine capable of performing measurements and deriving resultant waveforms. This engine supports multiple levels of expression, from low-level C code to an extended version of the ISPICE measurement language. The highest level of expression simplifies the process, making it easy to perform complex measurements directly at the command line. The waveform measurement engine can handle data from new and existing simulations.

Data Analysis Engine

JDE offers a data analysis engine with a complete set of data analysis and output processing filters that transform raw data into user-understandable forms. These filters can be executed from the command line or in scripts, and support a wide range of data manipulation operations. The seamless flow of data among JDE programs minimizes human error, simplifies the documentation of the development process, and makes iterative design changes easy. Result data can be expressed in various forms, including graphs, tables and formats suitable for inclusion in other simulations.

Characterization Flows

Characterization flows within JDE allow users to encapsulate all necessary information to characterize a design automatically and fully, even generating a report. Users can quickly iterate through design changes, viewing complete characterizations in minutes, thus gaining insights into circuit operations in less than an hour. This rapid turnaround gives unprecedented levels of insight in record time.

Schematic Prober and Analyzer

JDE includes a schematic prober and analyzer for multi-faceted schematic-based electrical checks, catering to users who want advanced JDE features using their existing, schematic-based environment. JDE remains compatible with any SPICE simulator. This ensures thorough electrical validation and extends the versatility of the JDE environment.

Foundry Model Support

JDE includes a unified library interface for access to all foundry SPICE models, which is automatically compiled directly from the foundry PDK. Sample libraries with 50 different TSMC model sets compile in as little as two minutes. The ready to use model libraries provide users quick access to all devices and with all model options. Basic device data such as supply voltage, channel length and fin width are in the library, and accessible to the JSPICE simulation and netlist.

User Accommodation

JDE is suited for a wide range of users, from experienced script writers to novices. Experienced users can encapsulate their complete characterization flows into generation scripts, allowing for automatic design characterization without remembering the details of the setup. Novice users can benefit from the simplified schematic-based electrical checks, which automate the simulation and validation processes.

The JDE Ecosystem and the Library

Open collaboration between users, content creators and service providers can spur innovation and dramatically reduce design time. While open collaboration is common in the world of commercial software, it is not common in the semiconductor industry. JDE hopes to change that by building a strong ecosystem that can populate libraries with rich content including useful modules or complete designs, data analysis utilities, easily modified characterization flows, and test suites for common protocols or applications. JDE users will also be able to draw on the community as well as ecosystem service providers with staffing and expertise. The future of semiconductors lies with universities that attract and train young engineering talent and JDE is well positioned to be their design environment of choice.

Conclusion

JDE significantly enhances the productivity of AMS circuit designers by providing major extensions to the SPICE language, advanced waveform analysis, parametric simulation sweeps, comprehensive data analysis, encapsulated characterization flows and schematic-based electrical checks. Using all available processor resources ensures fast results, making JDE an indispensable tool for modern engineers. By incorporating advanced features and a user-centric approach, JDE sets a new standard in AMS circuit design and simulation, enabling rapid and accurate design processes.

JDE™
JSPICE™ DESIGN ENVIRONMENT

John Maneatis is TCI's co-founder, President, and Chief Technologist. He holds a B.S. degree in Electrical Engineering and Computer Science from U.C. Berkeley, and M.S. and Ph.D. degrees in Electrical Engineering from Stanford University. John brings 36 years of experience to TCI in high-speed mixed-signal design, design automation and CAD software, and is world renowned for his work in the area of Phase-Locked Loop design. Prior to co-founding the company, he was a lead circuit designer at Silicon Graphics in their advanced microprocessor design group.

Brian Gardner is TCI's V.P. of Business Development. He is a long time semiconductor industry veteran, and has spent much of the last 25 years in the semiconductor IP market. He has held senior positions in general management, marketing and business development at Canaan, Denali, Cadence, QLogic and Motorola; as well as chip startups Interactive Silicon and OmegaBand. As General Manager of the microcontroller division at Motorola, he helped build the 68HC05 microcontroller into a dominant architecture with sales of more than three billion units. Brian holds a B.S. degree in Electrical Engineering from LSU.

True Circuits, Inc. is a leading provider of high-speed mixed-signal analog IP. It was founded in 1998 with headquarters in Los Altos. True Circuits builds easy to use, highly programmable hard macros, like Phase-Locked Loops, Delay-Locked Loops, and DDR PHYs, in most foundries and process variants. True Circuits has an experienced mixed-signal design team and close technical relationships with major foundries. Its customers include most semiconductor suppliers and design service providers. Over the 25 years that it has been in business, True Circuits has shipped countless IP blocks used on billions of chips in about 100 process variants.