TRUE CIRCUITS INC™

JDE™

JSPICE™ Design Environment

Summary

JDE™ is a powerful open design environment and ecosystem that greatly accelerates the creation of complex analog and digital circuits by enabling designers to explore, automate and innovate without restrictions or compromise.

Benefits

- Quickly define complex circuits
- Quickly define insightful measurements
- Quickly perform complete characterizations
- Run an **unlimited** number of simulations in parallel
- Automatically reduce results to key metrics
- Rapidly build intuition with quick feedback
- Utilize large library of circuits and generators
- Create circuits that are correct by construction

Features

- Simulate with all foundry models
- Simulate with Verilog-A, C or behavioral models
- Run delay-accurate mixed-mode simulations
- Perform logic/arithmetic synthesis
- Perform Monte Carlo and timing analysis
- Automatically place and route cells
- Configured for AWS™, Azure™, Google Cloud™

Ecosystem

- Collaborate with a community of other JDE users
- Share content, services and development effort
- Use open-source content or premium content
- Empower university students to pursue analog design
- Accelerate design at start-ups and research groups
- Utilize open-source and AI as technology enablers
- Build a community of explorers and innovators
- Make CAD budgets go further

Components

JSPICE Preprocessor
- Language processor
- Statistical timing analyzer

JSPICE Simulator
- Core simulator
- Netlist processing programs

JANA Sweep and Measurement Engines
- Simulation sweep engine
- Waveform measurement engine
- Data analysis engine

JCHAR Circuit Characterization Engine
- File processor compiler
- Characterization flows
- Logic gate characterization engine

JCLOUD Resource Connector
- Large-scale job controller
- Cloud process server
- Cloud file server
- General license server

JPROBE Schematic Prober and Analyzer
- Programmable definitions and flow control
- User- and pre-defined measurements

JLIBS Design Libraries
- Stimulus library
- Logic and arithmetic library
- Microprocessor library
- Synthesis function library
- Device model organization library

JDOCS Documentation and Application Notes
- Software installation guide
- User guide
- Cloud enablement guide
- Application notes

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Ecosystem and Enablement

ECOSYSTEM

A vibrant community of collaborators, from universities and businesses to individual designers, all providing content and services to make JDE the development environment of the future.

User Libraries and Community Content

A growing collection of complete designs, modules, generators, test suites, characterization flows, standard cells, all the things needed to accelerate circuit design and maximize productivity.

JDE Productivity Extensions

- Language Processor
- Measurement & Data Analysis
- Sweep and Job Control Engine
- Characterization Engine

Expressive netlist language with directed logic synthesis makes it easy to abstract designs into powerful design generators.

Sweep engine varies parameters and job control engine manages thousands to millions of simulations seamlessly.

Measurement and data analysis environment is packed with functions and reduces massive data into insightful information that builds intuition and encourages exploration.

Characterization engine allows user-specified characterization flows to be fully encapsulated and automated.

JSPICE Simulator

- Mixed-mode
- Massively Parallel
- Delay-accurate
- Cloud Enabled

Industry SPICE-compatible mixed-mode simulator with delay-accurate behavioral modeling, Verilog-A support, transient noise analysis, static timing analysis, multi-threaded execution, and full foundry SPICE model support.

Measurements can control stimulus and path simulations can simulate large designs quickly with SPICE-level accuracy.

Configured for AWS, Azure and Google Cloud for massively parallel simulations and 100X or more increases in real-world throughput.

Place and Route

- Directed P&R
- Design Generators

Placement data in the netlist source can direct P&R for high-speed designs.

Makes it easy to create process-independent designs.

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JDE makes it easy for users to rapidly design circuits. The key to rapid design is being able to quickly build intuition by iterating through changes and receiving quick and complete characterization feedback. JDE makes it easy to quickly define complex circuits, add structural options for testing, define insightful measurements, run complete characterizations over PVT and operating conditions in minutes, and automatically reduce the results to easily understood metrics. This enhanced understanding allows users to make definitive circuit changes that avoid optimization of a flawed design. Closing this iteration loop in minutes rather than hours or days is instrumental to rapid design.

JSPICE Language

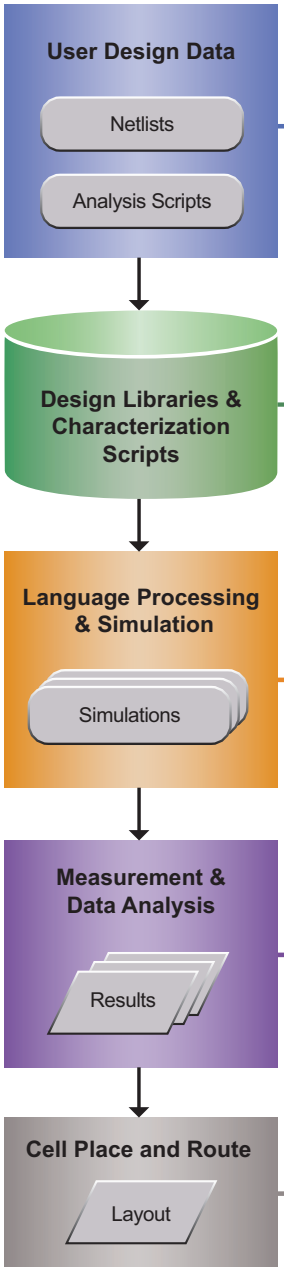
The JSPICE language is a dramatically extended version of generic SPICE circuit descriptions, which also includes optimized support for industry SPICE simulator syntax. While the language can be used with schematic capture, it essentially makes schematic capture obsolete for efficient design. The language adds both extended syntax and the C programming language to make statements surprisingly expressive and clear. It is compiled and supports precompiled objects for very fast access to large design libraries and data sets. It can generate not only generic SPICE output, but also Verilog, SDC constraints, LIB files, drive place and route flows for high-speed designs, and much more.

JSPICE Cloud Server

The JSPICE cloud server allows users to run single simulations or thousands, even millions, in parallel with no additional effort. The server handles the task of scheduling simulation processes and transferring files and data to both local and cloud compute resources seamlessly. Local compute resources can be used efficiently for small jobs, while the cloud resources will be automatically allocated as needed within the user-defined limits.

Typical Design Flow

JDE makes it easy to express complicated circuits, run a large set of simulations in parallel, perform complex waveform analysis and reduce the results to a form easily understood by the user, all leading to very rapid turnaround of circuit characterizations. A typical design flow is as follows:



All data needed for the design definition and testing is here.

Data analysis scripts utilize a large set of measurement and data reduction functions to simplify the automation of circuit characterization.

Design libraries contain logic and arithmetic circuits, stimulus and language extensions to simplify the expression of designs.

User- and pre-defined characterization scripts make it easy to automate circuit characterization.

The JSPICE language used in the design is preprocessed to create a very fast executable design generator.

Parallel simulations, one for each user-specified netlist parameter combination, are run locally or in the cloud.

Powerful waveform analysis language and data reduction programs distill data into human understandable results (numbers, plots, reports) and data to feed into other simulations.

High-speed analog and digital designs can be deterministically placed and routed allowing them to be process independent.

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Orders of Magnitude Faster Design

JDE enables users to achieve faster results by incorporating modern design and software technologies that greatly improve design productivity and encourage exploration and innovation.

Massively Parallel Simulation

JDE users can run massively parallel simulations, either locally or in the cloud, or both with **unlimited** JSPICE licenses. Users can sweep multiple parameters from min to max over all PVT corners, and JDE will create and manage those thousands of simulations and distill the results into the optimal design parameters.

Modern Text-Based Scripts and Programming

GUIs and schematics are a slow way to design. They resist automation. JDE incorporates text, processing code and scripts that move analog design into the realm of modern software. This will help attract young software-savvy talent to the field of analog design and result in further progress in design automation.

Cell-Based Design and Layout

JDE moves layout from mostly hand-drawn to cell-based without losing the layout control needed for critical circuits. The JDE design database contains placement information that allows routing to be done automatically. The bulk of the layout porting effort is thereby reduced to building and characterizing a set of cells.

Collaboration and the Ecosystem

Open collaboration between users, content creators and service providers can spur innovation and dramatically reduce design time. While open collaboration is common in the world of commercial software, it is not common in the semiconductor industry. JDE hopes to change that by building a strong ecosystem that can populate libraries with rich content including useful modules or complete designs, data analysis utilities, easily modified characterization scripts, and test suites for common protocols or applications. In addition to support and services from True Circuits, JDE users will also be able to draw on ecosystem service providers with the staffing and expertise to accelerate JDE adoption and ease-of-use. The future of semiconductors lies with universities that attract and train young engineering talent and JDE is well positioned to be their design environment of choice.

Membership Program

Individuals, students or employees of companies can submit a membership application by going to www.truecircuits.com/JSPICE. The application process will ask users to agree to the terms of the JDE membership program, including providing periodic feedback and participating in user forums. Users will be accepted by True Circuits, at its sole discretion, into the program for a selected period of time. Accepted users will be provided the JDE software suite, user guidelines, related documentation and a True Circuits point of contact for user support and feedback.

About True Circuits

True Circuits, Inc. offers a complete family of standardized, silicon-proven PLL, DLL and DDR PHY hard macros that spans nearly all performance points and features typically requested by ASIC, FPGA and SoC designers. True Circuits utilizes robust state-of-the-art circuits, a methodical and proven design and test strategy, and close associations with the major foundries. True Circuits' PLL, DLL and DDR PHY product portfolio is available in most TSMC, UMC and GLOBALFOUNDRIES processes and process variants from 180nm to 4nm.

Since 1998, True Circuits has distinguished itself as the technology leader in the timing IP space, and its PLLs and DLLs are used extensively around the world in its customers' products with production volumes in the billions.